PWM of Cascaded Five level Voltage Source Inverter using FPGA

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Abstract **- Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. Various topologies of multilevel inverter provides several advantages including lower voltage stress, higher efficiency, lower electromagnetic interference. To obtain a quality output voltage with minimum amount of ripple content, they require high switching frequency along with advance pulse width modulation strategies. As a result, a multilevel power inverter structure has been introduced as an alternative in high power applications.This paper presents single phase cascaded five level inverter with separate dc sources. Cascaded multilevel inverter constructed by two full H-bridges. FPGA is chosen for the hardware implementation of switching strategy mainly due to its high computation speed that can ensure the accuracy of the instants that gating signals are generated. VHDL language is used to model the inverter switching strategies.**

Index Terms - Cascaded H-bridge multilevel inverter, digital pulse width modulation(DPWM), field programming gate array(FPGA).

I.INTRODUCTION

Multilevel inverters have been attracting increasing attention in the past few years as power converters of choice in many applications. They have significant advantages over the conventional one because of the capability to reduce the undesirable harmonics in order to improve the performance and efficiency. It may be easier to produce a high power and high voltage inverter with multilevel structure because of the way in which device voltage stresses are controlled in structure.

Multilevel inverters are significantly different from the ordinary inverter where only two levels are generated. In which each group of devices contribute to a step in the output voltage waveform. The steps are increased to obtain an almost sinusoidal waveform. The number of switches involved is increased for every level increment. Generally the output waveform of the multilevel inverter is generated from different voltage sources obtained from the capacitor voltage sources. In the past two decades, several multilevel voltage source Multilevel Inverter for Single Phase System with Reduced Number of Switches converters have been introduced. The various topological structures of the multilevel inverter suggestions must cope with The following points: 1) less number of switching devices, 2) capable of enduring high voltage and high power, and 3) lower switching frequency for the switching devices. Cascaded H-bridge multilevel inverter is gaining faster development due to its topological and modularity significance.[1-3].

Ordinary PWM modulation for two-level inverters is accomplished through comparison between a reference wave and a triangular carrier wave. The reference wave have the frequency and amplitude wanted for the output voltage signal and the triangular carrier wave has the amplitude of half the DC input voltage, in an simple ordinary case, and its frequency is dependent on application but must be higher than the reference wave frequency.

Digital PWM generation is considered as an alternate modulation technique in place of the conventional sinusoidal PWM using triangular carriers for the multilevel inverter operation that has the advantages of implementation simplicity and possibility to reduce harmonic distortions. Some methods us carrier disposition and others use phase shifting of the multiple carrier signals. Digital controllers, such as microprocessors, DSP, FPGA and application specific integrated circuits (ASIC) are gaining importance in the power electronics applications as they can easily implement DPWM, with better performance and at low cost [4-8]. Therefore, digital control techniques are becoming more common solutions in modem power converters.Field Programmable Gate Array (FPGA) offers the most preferred way of designing PWM Generator for Power Converter Applications. FPGA is only an array of gate that can be connected as the user wishes. FPGA are used for relatively simpler operations but higher processing speed in comparison to microcontrollers. In the last few years, the field programmable gate array (FPGA) circuits have become popular in the applications where high performance, low development, low production cost and fast time-to market are required. We have to just change the interconnection between these logic blocks. This feature of reprogramming capability of FPGA makes it suitable to make your design using FPGA. Also using FPGA we can implement design within a short time and efficient hardware for rapid prototyping. Thus FPGA is the best way of designing digital PWM Generators. Also implementation of FPGA-based control schemes proves less costly and hence they are economically suitable for small designs.

II. OPERATION OF FIVE LEVEL CASCADED H-BRIDGE INVERTER

The cascaded H-bridge multilevel inverter circuit is shown in Fig. 1. The number of H-bridges required for an n-level inverter are N = (n-1)/2. Single-phase structure of the five level cascaded Hbridge inverter is shown in Fig. 1. The output phase voltage is equal to the summation of the output of the each H-bridge module as below.

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$$Vac = Vdc/2 + Vdc/2 + \ldots\ldots + Vmh \qquad (1)$$

Where h is the number of H-bridge modules used in the multilevel circuit.

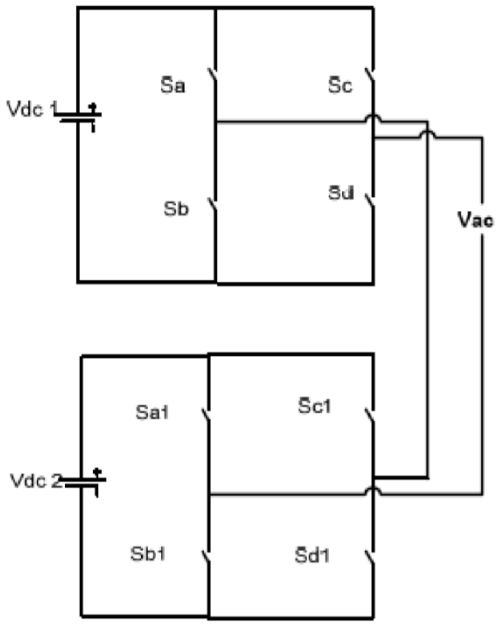

Figure.1. Cascaded 5 level MLI

S_{a1}	S_{b1}	S_{c1}	S_{d1}	S_a	S_b	S_c	S_d	V_{ac}
0	1	1	0	1	0	0	1	V_{dc}
0	1	1	0	1	0	1	0	$V_{dc}/2$
0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	0	$-V_{dc}/2$
1	0	0	1	0	1	1	0	$-V_{dc}$

Table.1 Switching Pattern of five level inverter

Each module of the H-bridge has its own input voltage and consists of four switching power devices; Sa, Sb, Sc, and Sd .Each module of the cascaded multilevel inverter can produce three levels of the output voltage which is +V, 0 and –V. This is made possible by connecting the DC sources sequentially to the AC side via four power devices. For example cascaded H-bridge multilevel inverter with four modules of the H bridge will produce nine levels of the output phase voltage.

The cascaded H Complete bridge multilevel inverter has several advantages because of its simple and modular circuit configuration. Each of its modules is identical and incorporates both input and output circuitry. Besides, the cascaded H-bridge multilevel inverter requires the least number of components compared to other types of multilevel inverter. These features provide flexibility in extending cascaded H-bridge multilevel inverter to higher number of levels without modification on the circuit itself.

III.PWMCONTROL OF MULTILEVEL INVERTER

The technique uses comparison of different carrier signals with the sinusoidal signal. The saw tooth waves as a carrier signals are used and generated by toolbox of the MATLAB/SIMULINK.

The power switch is usually of MOSFET or IGBT. . The modulation index is defined as: $M = Vm / 2Vc$ (2)

Where V_m is the peak value of digital sinusoidal wave and V_c is the carrier peak value [12]

Figure.2 Simulation of Single Phase Five Level Multilevel Inverter

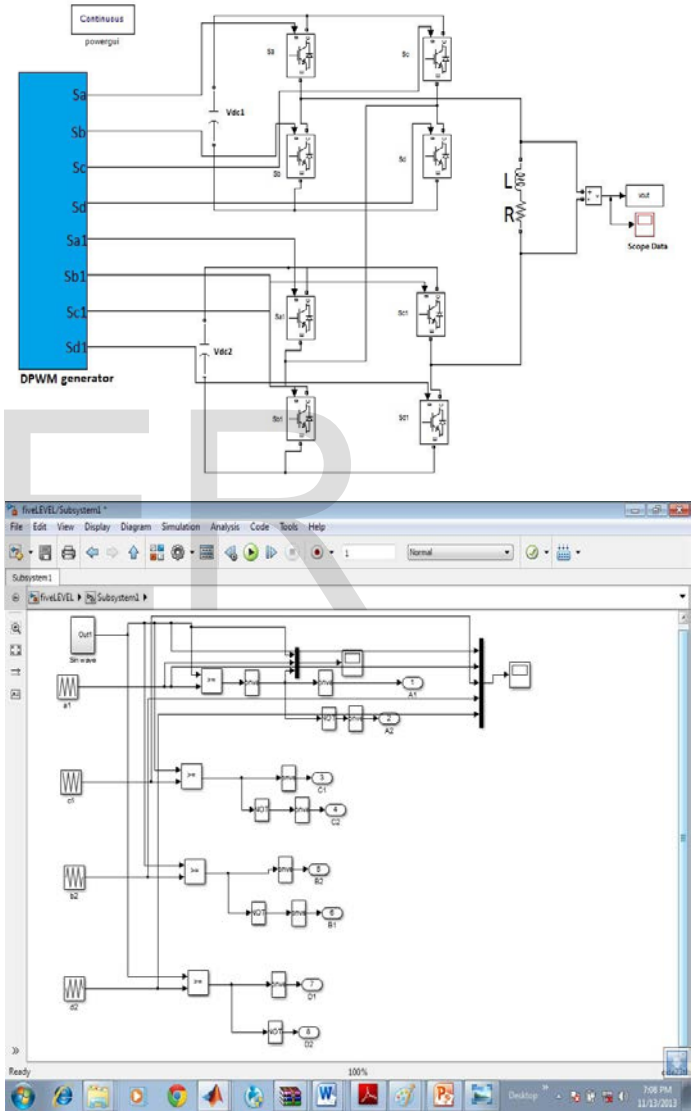

Figure 3.Subsystem in MATLAB/Simulink for PWM Gating signal generation.

SIMULATION RESULTS

The proposed five-level cascaded multilevel PWM single phase inverter is simulated by using MATLAB/Simulink. The different levels of the carrier signals (such as saw tooth signals) are compared with the sinusoidal (reference signal). Each saw tooth signal is of the same amplitude and same frequency of 1 kHz that is generated from the upcounter. The output voltage waveform of five-level cascaded H-bridge inverter has been simulated and shown in figure 4

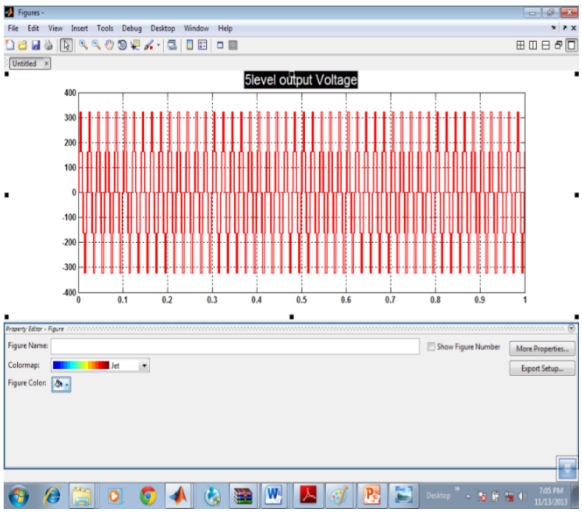

Figure .4.output voltage waveform of five-level cascaded H-bridge inverter

V. CONCLUSION

The FPGA based digital control switching patterns are adopted and applied to the cascaded multilevel inverter switches to generate multilevel output voltages. The FPGA reduces complexity, increases speed and adds flexible in the design of the control circuit for hardware implementation. It can efficiently extend the range of modulation index which facilitates a better quality output voltage with minimal distortion. The experimental, simulation and hardware implementation results demonstrate the improved quality voltage waveform shapes at the output of the inverter. The main objective of this thesis is to provide a general notion about the multilevel power converters and various modulation strategies mainly PWM techniques and their applications.

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